REMARKS

Claims 1 - 20 are pending in this application. Claims 12 - 20 are withdrawn from consideration as being directed to a non-elected invention. Claims 1 - 10 have been rejected and Claim 11 is objected to.

Applicants acknowledge, with appreciation, the Examiner's indication of the allowability of Claim 11, if rewritten in independent form. Accordingly, Claim 11 has been canceled and rewritten in independent form as new Claim 21.

Minor amendments have been made to Claim 1 to make the claim more readable. In addition, Claims 5, 7 and 9 have been amended to overcome the Examiner's objections in regard to the use of "A", as set forth in the specification, to represent Angstroms. Accordingly, the claims now use "Å", as suggested by the Examiner,

The 35 USC103 Rejection of Claims 1 - 7, 9 and 10

The examiner has rejected Claims 1 - 7, 9 and 10 under 35 USC103(a) as being unpatentable over Samavedam, et al. (USP6,423,632) in view of Fujiwara (USP6,301,155). In this rejection, it is apparently the Examiner's contention that the rejected claims read on Samavedam, et al. except for the "Si nano crystal layer" limitation in Claims 1 - 6 and the "Si nano crystal seed layer... with grain size less than 100Å" in Claims 7 - 10. For these latter limitations, the Examiner relies upon Fujiwara. However, it should be noted, that the Samavedam, et al., itself, is clearly deficient for reasons other than its failure to teach a "Si nano crystal layer".

The Samavedam, et al. Patent

The Samavedam, et al. patent is directed to polycrystalline silicon germanium alloy (SiGe) gate structures. As noted by the Examiner, Samavedam, et al. do not teach anything in regard to a Si nano crystal layer in their gate structure. However, in addition to not teaching anything in regard to a Si nano crystal layer, Samavedam, et al. also fail to teach anything in regard to a "thin interfacial oxide layer... sufficiently thin to cause minimum resistance to current flow and with sufficient [O] to block Ge" and where said interfacial oxide layer has "a thickness of 3 to 4Å" or is a "discontinuous" layer or a layer comprising "SiO_2 or $Si_xGe_yO_z$".

The Samavedam, et al. barrier layer is stated, in Col. 3, to be a "conductive portion" that may include "a metal or a metal with elements such as nitrogen, oxygen, and carbon such as metal nitride, metal carbide and/or a metal oxynitride and/or metal oxy-nitridecarbide". Contrary to the Examiner's reference to Col. 3, lines 29 - 47 of Samavedam, et al. for support, Samavedam, et al. do not teach "a thin interfacial oxide layer... sufficiently thin (3 to 4Å) to cause minimum resistance to current flow and with sufficient [O] to block Ge". Samavedam, et al. do not use [O] to block Ge but rather use a conductive layer 3 - 50 nanometers. Given the materials and material thickness range used by Samavedam, et al., this appears to be a totally different structure and mechanism for blocking Ge than that employed by Applicants.

To say, as the Examiner has stated, that the differences between Samavedam, et al. barrier layer and that claimed by Applicants is merely a matter of discovering the optimum or working ranges involving routine skill in the art is to fail to recognize the essential distinctions between the two approaches. There is no hint of a teaching or suggestion in Samavedam, et al. that Applicants' claimed barrier layer structure could be incorporated into Samavedam, et al. Moreover, it is not at all clear that Samavedam, et al. can physically reduce their barrier layer to 3 to 4Å, and if, indeed, they could, that Samavedam, et al. would even operate in the manner intended. For example, if the Samavedam, et al. layer were reduced to 3 to 4Å thick, it is not clear they would have a layer that would act as a barrier to Ge. It would seem that if their barrier could be that thin, they would have suggested a range to include it.

The Fujiwara Patent

Fujiwara is directed to a non-volatile memory device having a charge storing means as, for example, a floating gate in a floating gate type, a charge trap in a nitride film in a MONOS type device, a change trap near the interface between a top insulating film a nitride film, etc. In the MONOS type non-volatile memory transistor, a tunnel insulating structure using a nitride film acts to provide carrier traps that are used to hold charges for the memory function. In the Si-nano crystal non-volatile memory of Figure 11 of Fujiwara cited by the Examiner, a gate insulating film 30 takes the place of the nitride film 12 and top insulating film 14, and the Si-nano crystals 32 serving as dispersed charge storing means on the tunnel insulating film 10 and an oxide film 34 thereon are formed between gate electrodes.

The Examiner's Samavedam, et al./Fujiwara Combination Under 35 USC103

The Examiner states that Samavedam, et al. fail to teach the Si nano crystal seed layer formed on the SiO_2 insulating layer with the grain size of the Si nano crystal being less than 100Å. The Examiner goes on to state that Fujiwara teaches in Figure 11 a semiconductor device comprising "Si nano crystal 32 having a size of 10nm or less in diameter formed on a tunnel insulating film 10 (Col, 13, line 49 - Col. 14, line 50). The Examiner then concludes that "it would be obvious... to utilize the teaching of forming Si nano crystal having a size of 10nm or less in diameter on a tunnel insulating film to function as carrier traps made disperse in the planar direction (Col., 14, lines 22 - 23), as taught by Fujiwara to incorporate into and modify Samavedam's structure to arrive the claimed limitation".

Applicants are at a complete loss to see how the Si nano crystals on the tunnel insulating film of Fujiwara can be used in Samavedam, et al. Fujiwara discloses a non-volatile memory structure wherein the Si nano crystals act as charge storage means on a tunnel insulating film in a non-volatile memory structure.

Samavedam, et al. on the other hand, disclose a polycrystalline silicon germanium gate structure for current switching rather than non-volatile memory storage. Samavedam, et al. have no reason to employ Si nano crystals as charge storage means. In fact, to do so would be at cross-purposes to what Samavedam, et al. are trying to achieve. Samavedam, et al. do not want charge storage. To put non-volatile charge storage means in Samavedam, et al. would appear to render the Samavedam, et al. structure inoperative for its intended purposes. In fact, it is not clear to Applicants how Samavedam, et al. would, indeed, be modified given the tunnel insulating film/Si-nano crystal oxide memory structure of Fujiwara and the poly SiGe gate structure of Samavedam, et al.

Moreover, Applicants fail to see how one skilled in the art would be motivated to combine Fujiwara with Samavedam, et al. Clearly, there is no teaching or suggestion in either reference for making such a combination. It appears to Applicants that the Examiner has combined Fujiwara with Samavedam, et al. using Applicants' teachings in an effort to construct a device to anticipates Applicants' claimed invention and in so doing has rendered Samavedam, et al. inoperative.

Regarding the Examiner's rejection of Claim 9 on the Samavedam, et al./Fujiwara combination, Applicants' response is that same as that stated in regard to the Examiner's rejection of Claim 5.

The Samavedam, et al./Fujiwara/Yamamoto 35 USC 103(a) Rejection of Claim 8

The Examiner takes the position in this rejection that Samavedam, et al. and Fujiwara disclose all the claimed limitations except for the discontinuous interfaced layer SiO_2 or $Si_xGe_yO_z$. For the latter limitation, the Examiner relies upon Yamamoto.

Applicants have already pointed out the impropriety of combining Fujiwara with Samavedam, et al. The Examiner now extends this rejection to include using a barrier layer in Yamamoto. Apparently the Examiner suggests here that the barrier layer of Samavedam, et al. be replaced by the barrier layer 74 of Yamamoto. Given the vagaries of how the structure of Fujiwara would be combined with Samavedam, et al., it is not at all clear how Yamamoto would be included in the resultant structure of Samavedam, et al./Fujiwara. Moreover, it is not clear that if, somehow, all 3 references were combined, the Yamamoto barrier layer would be operative in Samavedam, et al. Applicants firmly believe that all of these suggested modifications are clearly more than a matter of obvious design choice. It appears that rather than a matter of design choice, the suggested modifications amount to constructing a new device to meet Applicants' claimed invention.

Summary

Applicants' claimed invention includes at least two limitations not taught by Samavedam, et al. The first of these is the "Si nano crystal layer" and the second is the "thin interfacial oxide layer... sufficiently thin (3 to 4Å) to cause minimum resistance to current flow and with sufficient [O] to block Ge". To meet the first limitation, the Examiner relies upon Fujiwara with Samavedam, et al. To meet the second limitation, the Examiner appears to overlook certain limitations and relies upon the position that the claimed thicknesses amount to discovering the optimum or working ranges involving only routine skill.

Samavedam, et al. is directed to a FET gate structure used to switch current while Fujiwara is directed to a floating gate non-volatile memory structure. The structure and the function of each are distinct from one another. There is nothing to motivate combining these references and, in fact, it would not make sense to combine them. Similarly, there would be no motivation for one skilled in the art to experiment with the thicknesses of the Samavedam, et al. barrier layer since the claimed barrier layer distinctions over Samavedam, et al. are a matter of both kind and thickness degree. One need only to look to the barrier layer thickness ranges suggested by Samavedam, et al. (3 - 50 nanometers and 10 - 30 nanometers) to confirm this point. Clearly, reducing the Samavedam, et al. barrier layer to the claimed barrier limitations involves much more than discovering optimum or working ranges.

Conclusion

Accordingly, in view of Applicants' amendment to the claims and remarks, Applicants firmly believe the application is now in condition for allowance. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the outstanding rejections, allow the claims as now presented, and pass the case to issue.

Respectfully submitted,

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